Remarks/Arguments:

Claims 1 through 22 are presently pending. As indicated below, although the Office Action Summary indicates that claims 1-22 are rejected, it is applicant's understanding that claims 1-6, 8-18, 21, and 22 are presently rejected and claims 7, 13, 19, and 20 are objected to. Applicant herein amends claims 7, 8, 13, and 14. No new matter is added. Applicant respectfully requests reconsideration in view of the above amendments and the following remarks.

Section 1 of the Office Action recites that "Claim 7 is objected to because of the following informalities: in line 3 'ones of' should be deleted" and that "Claim 13 is objected to because of the following informalities: in line 5 'ones of' should be deleted." Applicant has amended claims 7 and 13 herein in accordance with the Examiner's suggestion to further prosecution and to clarify the meaning of those claims.

Section 3 of the Office Action recites that "Claim 8 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement." Specifically, the Office Action recites:

> In line 3 the claim recites "first and second memory banks are not equal". However, the specification does not describe how two memory banks are made equal or not equal.

The phrase "not equal" indicates that the memory banks are "not the same." Applicants herein amend claim 8 (and also claim 14, which includes similar language) to recite "first and second memory bank are not the same memory banks." This is clearly enabled and supported in paragraph 44 of the application as originally filed. Applicant contends that claim 8 as amended is enabled and respectfully requests that the rejection of claim 8 under 35 U.S.C. 112 be withdrawn.

Section 4 of the Office Action and the Office Action Summary indicate that claims 1-22 are rejected. Specifically, the Office Action recites that "[c]laims 1-22 are rejected under 35 U.S.C. 102(a) as being unpatentable over Nystuen (2004/0088472) in view of Shiozaki et al. (4,683,533). Section 6 of the Office Action, however, indicates that "[c]laims 7, 19, and 20 are objected to . . . but would be allowable if rewritten in independent form." As section 4 of the

Office Action does not address claims 7, 19, and 20, it is assumed that the status of these claims is "objected to" rather than "rejected."

Applicant respectfully traverses the claim rejections for the reasons set forth below.

Nystuen is directed to a multi-mode memory controller. The multi-mode memory controller includes a bank control circuit that precharges memory banks in one of three operating modes. *See* Abstract of Nystuen.

Shiozaki is directed to a storage control system using plural buffer address arrays to track data transferred from a shared storage device into a buffer storage of a respective processor. The storage control system controls the update operations on two buffer address arrays. A first buffer address array includes a directory of buffer storage and a second buffer address array contains the same data as the first buffer address array. The storage control system updates the second buffer address array and then the first buffer address array of a processor in response to a block transfer of data from the shared storage device to a buffer of the processor and data stored to the shared storage device by other processors.

Claim 1 includes at least one feature that is not disclosed, taught, or suggested by Nystuen in view of Shiozaki. Claim 1 is directed to a memory controller and includes the following features (at least one of which is not found in the applied references):

> an arbiter configured to receive the memory requests from the plurality of requesters, the arbiter assigning a first memory request to a first processing path and a second memory request to a second processing path responsive to the memory banks requested by the received and assigned memory requests;
>
> a first path controller coupled to the arbiter and the plurality of memory banks, the first path controller configured to process the first memory request in the first processing path to activate a first memory bank associated with the first memory request;
>
> a second path controller coupled to the arbiter and the plurality of memory banks, the second path controller configured to process the second memory request in the second processing path to activate a second memory bank associated with the second memory request while the first memory bank is active; and

> a synchronizer coupled between the first path controller and the second path controller for synchronizing the first and second path controllers such that the first and second memory requests processed by the first and second path controllers, respectively, do not conflict.

This means that an arbiter receives memory requests and assigns the memory requests to a first path and a second path. A first path controller processes a request on the first path to activate a first memory bank and a second path controller processes a request on the second path to activate a second memory bank while the first memory bank is active. A synchronizer synchronizes the first and second path controllers such that the memory requests do not conflict.

The Office Action recites that Nystuen discloses:

> a memory controller for managing memory requests from a plurality of requesters to a plurality of memory banks, the memory controller comprising: an arbiter configured to receive the memory requests from the plurality of requesters, the arbiter assigning a first memory request to a first processing path and a second memory request to a second processing path responsive to the memory banks requested by the receive and assigned memory requests [Fig. 3; par. 3]; a first path controller . . . configured to process the first memory request in the first processing path to activate a first memory bank associated with the first memory request [Figs. 3 and 5; pars. 28-30]; [and] a second path controller . . . configured to process the second memory request in the second processing path to activate a second memory bank associated with the second memory request while the first memory bank is active [Fig. 1 and 3; pars. 23-28]. (Emphasis added.)

Applicant respectfully disagrees and submits that Nystuen clearly fails to disclose at least two of these features identified in the Office Action.

First, the arbiter in Nystuen assigns memory requests to a single path rather than two paths as called for in claim 1. As can be seen in Figure 3 of Nystuen, a request arbitration block 308 includes a single command signal path 334 over which requests can be passed to memory 302. Since there is only one path, the arbiter in Nystuen is incapable of assigning a second memory request to a second processing path. Further, Shiozaki fails to disclose, teach, or suggest this feature.

Second, Nystuen activates one memory bank at a time. As can be seen in Table 1 of Nystuen, a first bank (bank 0) is activated and written to prior to activating a second bank (bank 1). Likewise, each successive memory bank is activated and written to prior to activating the next successive memory bank. Thus, Nystuen fails to disclose, teach, or suggest a first path; a first path controller configured to process a first memory request in a first processing path to activate a first memory bank associated with the first memory request [Figs. 3 and 5; pars. 28-30]; [and] a second path controller . . . configured to process the second memory request in the second processing path to activate a second memory bank associated with the second memory request while the first memory bank is active. Further, Shiozaki fails to disclose, teach, or suggest these features.

Thus, the applied references (either alone or in combination) fail to disclose, teach, or suggest at least two features of claim 1. Accordingly, applicant respectfully request that the rejection of claim 1 be withdrawn.

Claims 9 and 15, while not identical to claim 1, includes features similar to claim 1. Accordingly, claims 9 and 15 are also allowable over the cited art for the reasons set forth above.

Claim 17 includes at least one feature that is not disclosed, taught, or suggested by the art of record. Claim 17 is directed to an arbitration method that includes the steps of:

> receiving the plurality of memory requests from the plurality of memory requesters during a current arbitration cycle;
>
> comparing the plurality of memory requesters to a grant history register identifying ones of the plurality of memory requesters that have had previous memory requests granted during the current arbitration cycle;
>
> assigning a memory request to one of the at least one controllers from the plurality of memory requesters not in the grant history register using fixed priority logic; and
>
> adding the requester of the assigned memory request to the grant history register.

In rejecting claim 17, the Office Action recites "the rationale in the rejection of claim 13 is herein incorporated." The rejection of claim 13 was based on Nystuen. Nystuen, however, fails to disclose, teach, or suggest at least the step of "assigning a memory request to one of

the at least one controllers from the plurality of memory requesters not in the grant history register using fixed priority logic." Nystuen does disclose a history register (i.e., history register 512). The history register in Nystuen, however, is used to determine when to precharge a memory bank rather than for purposes of assigning memory requests as called for in claim 1. Thus, Nystuen fails to disclose, teach, or suggest assigning a memory request to one of the at least one controllers from the plurality of memory requesters not in the grant history register using fixed priority logic. Likewise, Shiozaki fails to disclose, teach, or suggest this feature. Accordingly, applicant contends that claim 17 is allowable over the applied references and respectfully requests that the rejection of claim 17 be withdrawn.

Claim 21, while not identical to claim 17, includes features similar to claim 17. Accordingly, claim 21 is also allowable over the cited art for the reasons set forth above.

Claims 2-6, 8, 10-14, 16, 18, and 22 include all of the features of the independent claim from which they ultimately depend. Thus, claims 2-6, 8, 10-14, 16, 18, and 22 are also allowable over the cited references for at least the reasons set forth with respect to independent claims 1, 9, 15, 17, and 21. Accordingly, applicant contends that claims 2-6, 8, 10-14, 16, 18, and 22 are likewise allowable and, therefore, respectfully requests that the rejection of claims 2-6, 8, 10-14, 16, 18, and 22 be withdrawn.

Applicants acknowledge with appreciation the Examiner's finding that dependent claims 7, 19, and 20 include allowable subject matter and would be allowed if rewritten in independent form. Applicants submit, however, that there is no need to rewrite these claims in order to place them in condition for allowance because these claims are either directly or indirectly dependent on one of claims 1 and 17, which for the reasons discussed above, are also in condition for allowance.

In view of the amendments and remarks set forth above, applicant respectfully submits that claims 1-22 are in condition for allowance and early notification to that effect is earnestly solicited.

Respectfully submitted,

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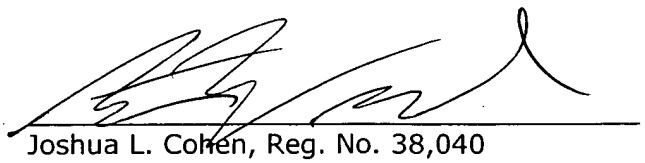

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The Director is hereby authorized to charge or credit Deposit Account No. **18-0350** for any additional fees, or any underpayment or credit for overpayment in connection herewith.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on June 23, 2006.

Kathleen P. Carney